WE CLAIM:

1. A static logic circuit on a SOI substrate, comprising:

a pull-up network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a circuit supply voltage which is connected to said first common node of said pull-up network;

a pull-down network which is connected to said second common node of said pull-up network; and

an output node which is connected to said second common node of said pull-up network.

2. The static logic circuit of claim 1 wherein said pull-down network comprises a plurality of series connected MOS transistors connected to a circuit ground.

3. The static logic circuit of claim 2 wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor.

4. The static logic circuit of claim 1 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

5. The static logic circuit of claim 2 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

6. A static logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a circuit ground which is connected to said first common node of said pull-down network;

a pull-up network which is connected to said second common node of said pull-down network; and

an output node which is connected to said second common node of said pull-down network.

7. The static logic circuit of claim 6 wherein said pull-up network comprises a plurality of series connected MOS transistors connected to a circuit supply voltage.

8. The static logic circuit of claim 7 wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor.

9. The static logic circuit of claim 6 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

10. The static logic circuit of claim 7 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

11. A static logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node;

a circuit ground which is connected to said first common node of said pull-down network;

a pull-up network which is connected to said second common node of said pull-down network; and

an output node which is connected to said second common node of said pull-down network.

12. The static logic circuit of claim 11 wherein said pull-up network comprises a plurality of series connected NMOS transistors connected to a circuit supply voltage.

13. The static logic circuit of claim 11 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

14. The static logic circuit of claim 12 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

15. A static logic circuit on a SOI substrate, comprising:

a pull-up network comprising a plurality of parallel connected NMOS transistors with a first and second common node;

a circuit supply voltage which is connected to said first common node of said pull-up network;

a pull-down network which is connected to said second common node of said pull-up network; and

an output node which is connected to said second common node of said pull-up network.

16. The static logic circuit of claim 15 wherein said pull-down network comprises a plurality of series connected PMOS transistors connected to a circuit ground.

17. The static logic circuit of claim 15 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

18. The static logic circuit of claim 16 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.